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MEMORY EXPANSION AND CHIP SCALE STACKING SYSTEM AND METHOD

Abstract

The present invention stacks chip scale-packaged integrated circuits (CSPs) into modules that conserve PWB or other board surface area. In another aspect, the invention provides a lower capacitance memory expansion addressing system and method and preferably with the CSP stacked modules provided herein. In a preferred embodiment in accordance with the invention, a form standard is disposed between the flex circuitry and the IC package over which a portion of the flex circuitry is laid. In a preferred embodiment, the form standard will be devised of heat transference material such as copper to improve thermal performance. In a preferred embodiment, a high speed switching system selects a data line associated with each level of a stacked module to reduce the loading effect upon data signals in memory access. This favorably changes the impedance characteristics exhibited by a DIMM board populated with stacked modules. In a preferred embodiment, FET multiplexers for example, under logic control select particular data lines associated with particular levels of

stacked modules populated upon a DIMM for connection to a controlling chip set in a memory expansion system.